Non-Volatile Settings

Application note: Change permanent device settings

The Pure Photonics tunable laser loads the setpoints for power, frequency and several other parameters from memory, upon startup. The customer accessible settings can be saved to the memory, so that after restart, the setpoints are changed. This is particularly useful to set the laser to a specific frequency and power.

This application note describes the process to change those settings and the parameters affected.

1. Process for saving non-volatile parameters

The process of saving the non-volatile parameters is to configure the device with the desired parameters and then trigger the save to memory through the genCfg register (0x08). We recommend to power-cycle the device before this process, to make sure that there are no unintended changes made prior to the process and we recommend a power cycle afterwards.

In this section we describe the process through the Pure Photonics CLI (Command Line Interface), which is available for download on the Pure Photonics website (support section). And we provide the raw RS-232 commands (hexadecimals). We include an example of setting power (to 12.32dBm) and frequency (to 193.41THz), but other parameters can also be set.

	CLI	**RS-232**
Reset laser		
Connect to laser	it.connect(1,9600) #for COM port 1	Open serial port
Set Power to 12.32dBm	it.pwr(1232)	0x A1 31 04 D0 (0x04D0=1232)
Set frequency to 193.41THz	it.fcf1(193) it.fcf2(4100)	0x A1 35 00 C1 (0xC1=193) 0x 11 36 10 04 (0x1004=4100)
Save Settings	it.genCfg(sdc=1)	0x 11 08 80 00 (bit 15 = 1)
Reset laser		

The genCfg register is defined in the MSA as follows:

Data Value Description

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDC	0x0000														

Bit 15: SDC (Store default configuration)

Read: Always returns zero.

Write:

"1": Save all non-volatile module configuration values in non-volatile memory. This bit is self clearing. Upon power on or hard reset, the module

2. Parameters saved

Parameter	Register	Details
IOCap	0x0D	See below
Fatal Power Threshold	0x22	In units of 0.01dB
Warning Power Threshold	0x23	In units of 0.01dB
SRQ Triggers	0x28	See below
Fatal Triggers	0x29	See below
Alarm Triggers	0x2A	See below
Channel	0x30	1 and up
Optical Power Set Point	0x31	In units of 0.01dBm
Module Configuration Behavior (MCB)	0x33	See below
Grid Spacing	0x34	In units of 100MHz
First Channel Frequency [THz]	0x35	In units of THz
First Channel Frequency [100MHz]	0x36	In units of 100MHz
Fatal Age Threshold	0x5F	In units of %
Warning Age Threshold	0x60	In units of %
Fine Tune Frequency	0x62	In units of MHz

IOCap Details

The IOCap register has the following format and assumes default values upon power up or hardware reset.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0			RMS	0x0			Reserved (0x0)	Current Baud Rate				Supported Baud Rates			

Bits 0-3 – Maximum baud rate supported by the module[20]. (Not writable)

0x00 – 9600
0x01 – 19200
0x02 – 38400
0x03 – 57600
0x04 – 115200
0x05 – 0x0F – Undefined

Bits 4-7 – The module's currently configured baud rate (writable) (default 0x00)

0x00 – 9600
0x01 – 19200
0x02 – 38400
0x03 – 57600
0x04 – 115200
0x05 – 0x0F – Undefined

Bit 8 – Reserved (0x0).

Bits 9-11 Reserved

Bits 12 – RMS - Configurable action upon low to high transition of MS*

0x0 – Baud rate will be reset to default (0x00) and input buffer cleared upon low to high transition of MS* (default).

0x1 – Clear the input buffers but do not reset the baud rate.

Bits 14-15 – Reserved (default 0x00)

SRQ Triggers details

A "1" bit signifies that the corresponding status register bit triggers the assertion of the SRQ* line. A "0" signifies that the corresponding status register bit does not trigger the assertion of the SRQ* line.

The layout of the SRQT register follows the same format as the status registers (StatusF, StatusW 0x20, 0x21).

15	14	13	12	11	10	9	8
			DIS	WVSFL	WFREQL	WTHERML	WPWRL
0	0	0	1	1	1	1	1

7	6	5	4	3	2	1	0
XEL	CEL	MRL	CRL	FVSFL	FFREQL	FTHERML	FPWRL
1	0	1	1	1	1	1	1

FATAL Triggers details

A "1" bit signifies that the corresponding status register bit triggers the assertion of the FATAL condition. A "0" signifies that the corresponding status register bit does not trigger the assertion of the FATAL condition.

The layout of the FatalT register follows the same format as the status registers (StatusF, StatusW 0x20, 0x21). This register sets the bits for which the FATAL condition is asserted. It follows the similar format as the status register (0x20, 0x21).

15	14	13	12	11	10	9	8
				WVSFL	WFREQL	WTHERML	WPWRL
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
		MRL		FVSFL	FFREQL	FTHERML	FPWRL
0	0	0	0	1	1	1	1

The FATAL condition can be de-asserted by either changing this register or by clearing the latched fault condition in the status registers (0x20).

ALARM Triggers details

A "1" bit signifies that the corresponding status register bit triggers the assertion of the ALM condition. A "0" signifies that the corresponding status register bit does not trigger the assertion of the ALM condition.

The layout of the ALMT register follows the same format as the status registers (StatusF, StatusW 0x20, 0x21).This register sets the bits for which the ALM condition is asserted. It follows the similar format as the status register (0x20, 0x21).

15	14	13	12	11	10	9	8
				WVSF	WFREQ	WTHERM	WPWR
0	0	0	0	1	1	0	1

7	6	5	4	3	2	1	0
				FVSF	FFREQ	FTHERM	FPWR
0	0	0	0	1	1	0	1

A setting of 0x0700 which is useful (along with ADT in the Module configuration register (MCB 0x33) to cause the ALM status to function as a LOCKED indicator. ALM is then asserted during tuning or output disable. The ALM condition can be de-asserted by changing this register.

MCB details

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000													SDF	ADT	0

Bit 1: ADT – Alarm during tuning or disable (warning status flags)
The default (0x1) allows alarm conditions during tuning or disable. If set to 0x1, ALM is asserted during tuning or when the output is disabled. This default causes the ALM status to function as a LOCKED to channel indicator, even during tuning. Note that ALMT (0x2A) should be set to at least 0x0700 for this behavior.

Bit 2: SDF – Shut down optical output on fatal condition.
A fatal condition occurs when the FATAL is asserted.
The default (0x0) does not cause the optical output to shutdown on fatal alarm.
Fatal conditions are somewhat technology specific but would be signaled by any of the bits 10:8 in register 0x20 (StatusF) being set.